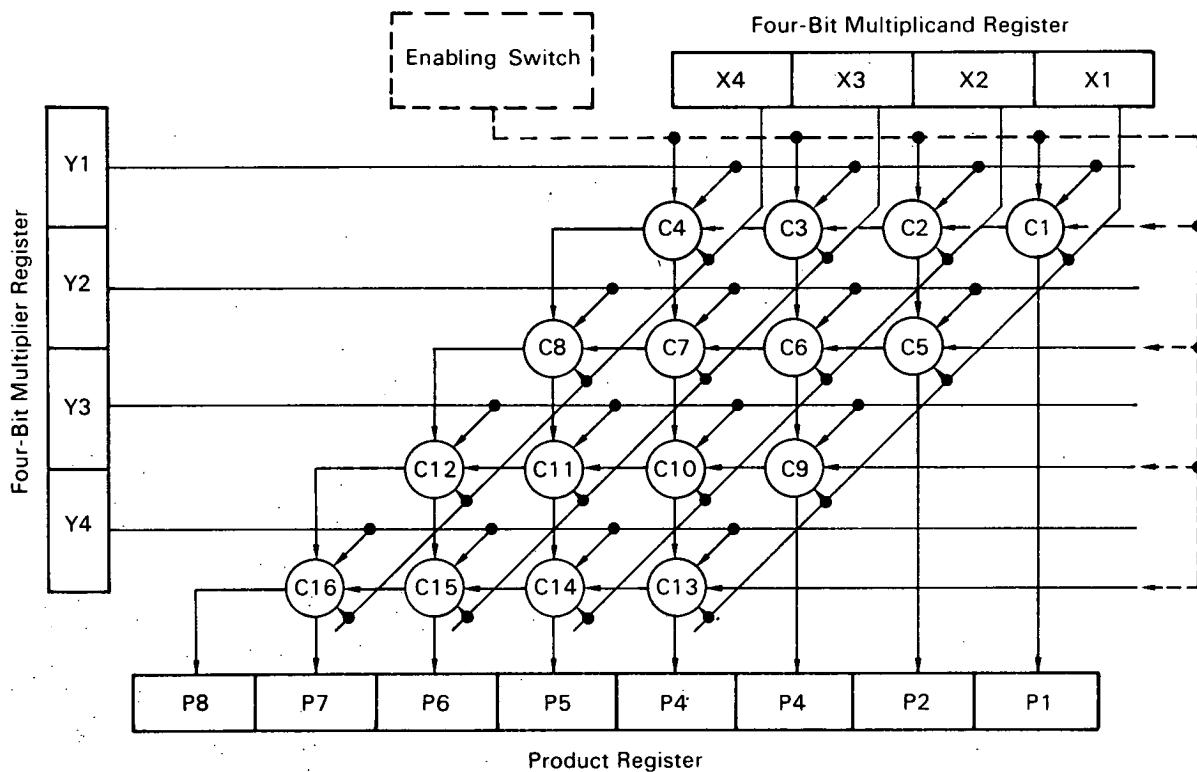


# NASA TECH BRIEF



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## Array Multiplier



### The problem:

To design a modular multiplier for use in computer applications of airborne vehicles, utilizing Large Scale Integration (LSI) and Metal Oxide Semiconductors (MOS).

### The solution:

Use a digital array multiplier consisting of, any number of identical digital adder cells in a repetitive planar configuration.

### How it's done:

For simplicity, a  $4 \times 4$  array multiplier is illustrated in the figure. Sixteen logic cells (C1-C16) are arranged in 4 rows of 4-bits each and correspond to the partial products as dictated by the corresponding multiplier bits. In the array network, the 4-bit multiplicand is stored in the uppermost register of the figure. The 4-bit multiplier is stored in the register at the left of the figure. The product is stored in the 8-bit register at

(continued overleaf)

the bottom of the array. All unused inputs, such as the rightmost carry-in and the topmost sum lines, are set into the logical "0" state by the enabling switch. Doing this prevents noise from disturbing the operation.

Physically, each bit of the multiplicand (X1, X2, X3, X4) is coupled to a cell element of the partial product row for all rows in the corresponding bit position: X1 is coupled to cells C1, C5, C9, and C13. Each multiplier bit (Y1, Y2, Y3, Y4) is coupled to all cell elements of the corresponding partial product row in parallel. The array operates asynchronously, and as long as there are multiplier and multiplicand bits in the X and Y registers, the array will continue accumulating the partial products. After a short time delay for propagating carries, the final product is available at the product register.

#### Note:

Requests for further information may be directed to:  
Technology Utilization Officer  
Headquarters  
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Reference: TSP70-10047

#### Patent status:

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